Comparative Analysis of Two Zero-Current Switching Isolated DC-DC Converters for Auxiliary Railway Supply

POLYTECH.MONS

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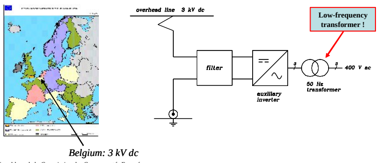
Contents

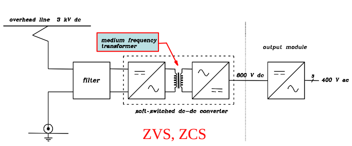
Context

- Currently the electrical separation between the HVS (3 kV dc) and the consumers side at each output port of the APS system of the auxiliary equipments is realized by heavy and bulky 50 Hz transformers



Doc. Livre blanc de la Commission des Communautés Européennes : « La politique européenne des transports à l'horizon 2010 : l'heure des choix » (http://www.info-europe.fr/doc02/248/g000f17f.pdf)

- New APS are considered that consist in soft-switched dc-dc converters and diverse output modules supplied by a common 600 V dc intermediate circuit
- Input and ouput sides are electrically separated by a lightweight medium-frequency (MF) transformer (typ. several kHz)



- Comparative analysis between two different topologies of HB-ZCS-PWM dc-dc converters

Operating conditions

- Proposed solutions, using 6.5 kV IGBTs, should meet the requirements of operating conditions listed below:

TABLE I
OPERATING CONDITIONS

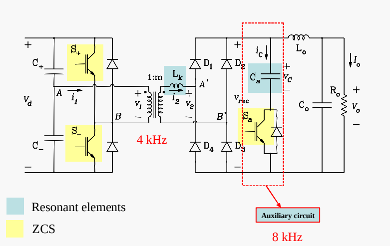
Maximum output power	P_o	100 kW
DC input voltage	V_d	2 ~ 4 kV
DC output voltage (regulated)	V_o	600 V
Load current	I_o	0 ~ 333 A
Switching frequency	f_s	4 kHz

Input voltage subject to wide variations

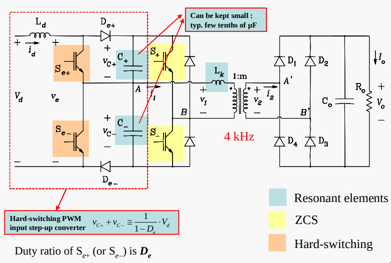
No load up to twice the rated current (at 3 kV input)

Medium frequency

First topology



Second topology



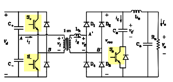
Duty ratio of S_{e+} (or S_{e-}) is D_e

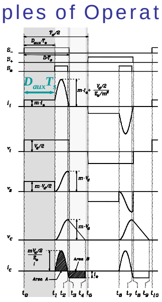
$$v_{C+} + v_{C-} \cong \frac{1}{1-D_e} \cdot V_d$$

Comparison criteria

1. Number of components
2. Ratings of power semiconductor devices
3. Size and weight
4. Total power losses (conduction and switching) in power semiconductor devices
5. Proper operation in the whole range of dc input voltage
6. Operation in the whole range of load

Topology #1: Principles of Operation



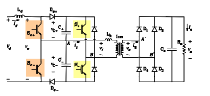


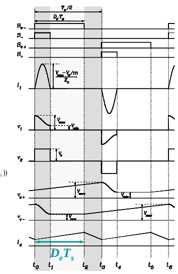
- **Mode 1.** Operation is just the same as for a conventional hard switching PWM HB converter
- **Mode2.** S_a turns ON, resonance starts

$$v_C = \frac{mV_d}{2}\left[1-\cos\left(\omega_0\left(t-t_1\right)\right)\right] \qquad i_2 = I_o + \frac{mV_d}{2Z_0}\sin\left(\omega_0\left(t-t_1\right)\right)$$

- **Mode 3.** Capacitor current (i_C) reverses and flows through the anti-parallel diode of S_a. S_a is turned OFF with ZCS
- **Mode 4.** Secondary current (i_2) reduces to zero and cannot change direction. Reflected current in the primary side is (i_1) cancelled in S_-. S_- is turned OFF with ZCS
- **Mode 5.** C_a is completely discharged. Output current I_o freewheels through D_1~D_4.

Topology #2: Principles of Operation





Continuous conduction in L_d

- **Mode 1.** S_{e-} and S_- are both turned ON, resonance starts between L_k and C_-. Current in L_d increases linearly, C_+ is charged linearly.

$$v_{C-} = V_{max} - \left(V_{max} - \frac{V_o}{m}\right)\cdot\left[1-\cos\left(\omega_0\left(t-t_1\right)\right)\right] \qquad i_1 = \frac{V_{max} - V_o/m}{Z_0}\sin\left(\omega_0\left(t-t_1\right)\right)$$

- **Mode2.** Primary current (i_1) decreases to zero at $t=t_1$. S_- is turned OFF with ZCS. C_+ is still charged linearly as the path (S_{e-}, D_{e+}) remains on. v_{C-} is clamped to V_{min}. D_1~D_4 are all turned OFF.
- **Mode 3.** This mode is characterized by the sole conduction of the diodes D_{e+} and D_{e-}. Current in L_d decreases linearly, C_+ and C_- are charged linearly

Topology #2: Steady-State Output Voltage Characteristics

- Continuous conduction in L_d
- If S_{e-} remains ON longer time than S_-, i.e. $D_e > D_{e,\min}(=k/2)$:

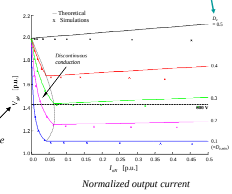
$$V_{oN} = \frac{1}{1-D_e} + m^2\pi\frac{D_e - D_{e,\min}}{2k}\cdot I_{oN}$$

$$k = \frac{\omega_s}{\omega_0} = \frac{\text{switching frequency}}{\text{resonant frequency}}$$

Voltage conversion ratio of input step up converter

Normalized output voltage

Control variable D_e



Normalized output current

Topology #1: Steady-State Output Voltage Characteristics

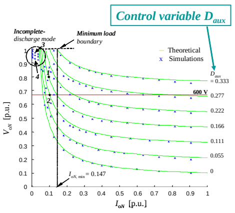
- If C_a is completely discharged before $t=T_s/2$:

$$V_{oN} = \frac{2}{T_s}\int_{t_0}^{t_0+T_s/2} v_{recN}(t)\cdot dt = 2D_{aux} + \frac{k}{\pi}\left[(\alpha+\pi) + I_{oN} + \frac{(\cos\alpha+1)^2}{2I_{oN}}\right]$$

$$k = \frac{\omega_s}{\omega_0} = \frac{\text{switching frequency}}{\text{resonant frequency}}$$

Normalized output voltage

Control variable D_{aux}



Normalized output current

- Topology #1 is not able to supply 600 V at light loads
- A solution consists in making the auxiliary circuit inoperative ? S_+ and S_- achieve hard swiching

Topology #2: Operation at No Load

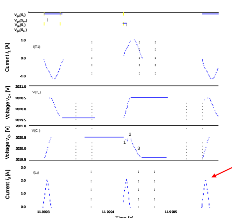
- At no load, S_{e-} remains ON less time than S_-, i.e. $D_e < D_{e,\min}(=k/2)$:

Primary current (i_1)

Voltage across capacitor C_+ (v_{C+})

Voltage across capacitor C_- (v_{C-})

Current through inductor L_d (i_d)



Simulation results with Saber

Comparison

Number of components

- Topology #1: 3 switches, 4 diodes, 7 passive components (including MF transformer)
- Topology #2: 4 switches, 6 diodes, 5 passive components (...)

Ratings of power semiconductor devices

TABLE II
POWER SEMICONDUCTOR DEVICES AND RATED SPECIFICATIONS

	Power devices	Part number	Rated voltage [kV]	Rated current [A]
Topology #1	S_+, S_-	FZ 200 R65 KF1	6.5	200
	S_a	FF 200 R33 KF2C	3.3	200
	D_1 ~ D_4	DD 400 S33 K2C	3.3	400
Topology #2	S_{e+}, S_{e-}	FZ 1200 R33 FF2C	3.3	1200
	D_{e+}, D_{e-}	DD 200 S33 K2C	3.3	200
	S_+, S_-	FZ 200 R65 KF1	6.5	200
	D_1 ~ D_4	BYM 300A 120 DNZ (2 in parallel)	1.2	2×300

Primary switches have the same ratings

Input step up converter increases the global power rating

Size and weight

TABLE III
CURRENT AND VOLTAGE RATINGS IN THE TRANSFORMER

	Current [A]				Voltage [V]			
	i_1		i_2		v_1		v_2	
Topol.	rms	peak	rms	peak	rms	peak	rms	peak
#1	167	585	278	976	1301	2000	830	2268
#2	241	761	862	2717	1020	2587	282	618

Requirements in terms of current is significantly less for Topology #1

Yet, the overall size and weight reduction gain is expected to be rather **in favour of Topology #2.** Qualitative reasons for that are:

- Topology #1 includes *two additionnal passive components* (C_r and L_o)
- Input inductor L_d is expected to be smaller in Topology #2 due to the *interleaved* input current ripple drawn by the primary step-up converter $2xf_s$
- Due to connection between input step-up converter and HB inverter in Topology #2, the *common capacitance value of the capacitors leg can be kept very low*

Total power losses in power semiconductor devices

TABLE IV
LOSSES IN POWER SEMICONDUCTOR DEVICES AT RATED INPUT VOLTAGE AND FULL LOAD CONDITION

	Power devices	Losses [W]	Total loss [W]
Topology #1	S_+, S_-	2× 166.3	1159.7
	S_a	134.3	
	D_1 ~ D_4	4× 173.2	
Topology #2	S_{e+}, S_{e-}	2× 887.8	3337.6
	D_{e+}, D_{e-}	2× 51.8	
	S_+, S_-	2× 142.8	
	D_1 ~ D_4	8× 146.6	

Total power loss is significantly less for Topology #1 (no hard-switching

- Conduction losses

$$P_{on} = V_{th}\cdot I_{ave} + r\cdot I_{rms}^2$$

- Hard-switching losses

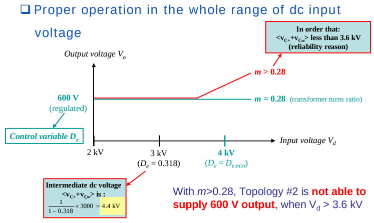
$$P_{sw} = f_s\cdot\left(E_{turn-on} + E_{turn-off}\right)_{T_j, I_C, V_{CE}}$$

- Soft-switching losses and diodes turn-off recovery losses are ignored

Operation in the whole range of load

- Topology #1: YES but it is necessary to adapt the control scheme at light load making the auxiliary circuit inoperative (hard-switching)
- Topology #2: YES it is inherently able to operate correctly from no load to the maximum load of the power supply, provided that D_e is reduced below $D_{e.min}$

Proper operation in the whole range of dc input voltage



With m>0.28, Topology #2 is **not able to supply 600 V output**, when V_d > 3.6 kV

Conclusion

Comparison

	Topology #1	Topology #2
Global power rating of power semiconductor devices	●	
Overall weight and size reduction of passive components		●
Total power loss of power semiconductor devices	●	
Operation in the whole range of dc input voltage	●	
Operation in the whole load range	●	●

● *strengths*